

Zen PPU Debug — Datasheet

Automotive Ethernet MAC + TSN — Datasheet (DSHT-00-INDEX)

The product DATASHEET for the Zen Automotive Ethernet MAC + TSN (zen-aveth-kit-v1, Wave-B **flagship**) — an IEEE 802.3 MAC with 802.1Qbv time-aware shaping, 802.1Qav credit-based shaping, and 802.1AS/1588 PTP timestamping, on the struct-typed peripheral bus. This is the **row-1 hub** of a hierarchical, multi-file datasheet. Product/integrator-facing. Instantiated from shared-agent-infra/DATASHEET-STANDARD.md. Product altitude — *what it does + how to integrate*, not *how it's built*. = outline · = authored (pending review) · = content complete + reviewed.

What this datasheet is (and is not)

- **Is:** the product datasheet — features, standards compliance, TSN operating model, interfaces, programming model, register map, performance, integration/deliverables.
- **Is not:** the design spec (DS-NN), μ Arch (UARCH), or DV testplan (DV-NN). Distilled from the as-built RTL (rtl/aveth/zen_aveth.sv); **RTL wins** on structural disagreement.
- **Altitude:** *what it does + how to integrate*. Uncharacterized numbers marked **TBC** with an owner.

How to read it

- Start at [\[\[docs/datasheets/aveth/DSHT-01-OVERVIEW|DSHT-01\]\]](#); TSN users go to [\[\[docs/datasheets/aveth/DSHT-05-FUNCTIONAL-OVERVIEW|DSHT-05\]\]](#) + [\[\[docs/datasheets/aveth/DSHT-10-REGISTER-MAP|DSHT-10\]\]](#).
- **Numbers policy:** every quantitative spec is sourced (RTL/register-map), a standards requirement, or marked **TBC** with an owner.

Chapter map

DSHT	Chapter	Scope	Sour (DS/DV/U
[[docs/datasheets/aveth/DSHT-00-INDEXIDSHT-00]]	Intro & TOC	this hub	—
[[docs/datasheets/aveth/DSHT-01-OVERVIEWIDSHT-01]]	Product overview	positioning · target apps · block diagram	rtl/aveth · [[docs/kits/LICENSE-
[[docs/datasheets/aveth/DSHT-02-FEATURES-COMPLIANCEIDSHT-02]]	Key features & standards compliance	802.3 / Qbv / Qav / 802.1AS matrix	rtl/aveth
[[docs/datasheets/aveth/DSHT-03-APPLICATIONSIDSHT-03]]	Applications / use models	zonal / SOA backbone	—
[[docs/datasheets/aveth/DSHT-04-CONFIGURABLE-OPTIONSIDSHT-04]]	Configurable options	parameters	rtl/aveth (p
[[docs/datasheets/aveth/DSHT-05-FUNCTIONAL-OVERVIEWIDSHT-05]]	Functional overview	MAC · TAS shaper · CBS · PTP	rtl/aveth
[[docs/datasheets/aveth/DSHT-06-INTERFACES-SIGNALSIDSHT-06]]	Interfaces & signals	MII · bus · IRQ	rtl/aveth (p
[[docs/datasheets/aveth/DSHT-07-CLOCKING-RESETIDSHT-07]]	Clocking & reset	clock/reset · PTP time base	rtl/aveth
[[docs/datasheets/aveth/DSHT-08-POWER-ON-RESET-INITIDSHT-08]]	Power-on / reset / init	bring-up ordering	rtl/aveth
[[docs/datasheets/aveth/DSHT-09-PROGRAMMING-MODELIDSHT-09]]	Programming model	TX/RX · GCL · CBS · PTP sequences	rtl/aveth
[[docs/datasheets/aveth/DSHT-10-REGISTER-MAPIDSHT-10]]	Register map	full CSR map	rtl/aveth (F
[[docs/datasheets/aveth/DSHT-11-PERFORMANCEIDSHT-11]]	Performance	throughput/latency · PTP resolution	rtl/aveth
[[docs/datasheets/aveth/DSHT-12-PHYSICALIDSHT-12]]	Physical / implementation	area/fmax	TBC
[[docs/datasheets/aveth/DSHT-13-RASIDSHT-13]]	RAS & data integrity	FCS · counters · error reporting	rtl/aveth
[[docs/datasheets/aveth/DSHT-14-VERIFICATION-DELIVERABLESIDSHT-14]]	Verification & deliverables	TB · manifest	verif · [[docs/kits/LICENSE-
[[docs/datasheets/aveth/DSHT-15-INTEGRATION-GUIDEIDSHT-15]]	Integration guide	MII/PHY · tie-offs · DFT	rtl/aveth
[[docs/datasheets/aveth/DSHT-16-ORDERING-LICENSINGIDSHT-16]]	Ordering / licensing / support	commercial	[[docs/kits/LICENSE-
[[docs/datasheets/aveth/DSHT-A-APPENDICESIDSHT-A]]	Appendices	signals · acronyms · revision history	—

Moniker & provenance

- **Moniker DSHT** per shared-agent-infra/DATASHEET-STANDARD.md. Path: docs/datasheets/aveth/DSHT-NN-NAME.md.
- **Provenance:** distilled from rtl/aveth/zen_aveth.sv (MAC + TAS + CBS + PTP register block) + the AVETH license kit. RTL wins on structural disagreement.

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DSHT-01 · Product Overview

Scope. What the Zen Automotive Ethernet MAC + TSN is and its headline characteristics. Product altitude. Distills rtl/aveth/zen_aveth.sv + [[docs/kits/AVETH-LICENSE-KIT|kit]].

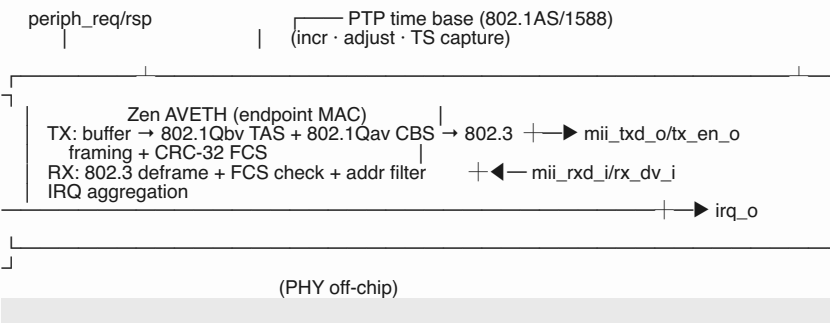
Overview

- The **Zen AVETH** is an IEEE 802.3 Ethernet **MAC** endpoint with an integrated **TSN** feature set: a **802.1Qbv** time-aware shaper (gated queues on a gate-control list), a **802.1Qav** credit-based shaper, and **802.1AS / 1588 PTP** hardware timestamping.
- It is the **zonal / service-oriented-architecture backbone** for automotive SoCs: bounded-latency scheduled traffic plus a network-wide PTP time base. CAN/LIN/SENT/FlexRay bridge onto it.
- MII datapath (8-bit) to an **off-chip PHY**; this is an **endpoint MAC**, not a switch. Attaches via the struct-typed peripheral bus.

Key specifications (at a glance)

Characteristic	Value	Source
MAC	IEEE 802.3 framing + CRC-32 FCS, address filter, loopback	RTL (SOURCED)
Time-aware shaper	802.1Qbv gate-control list (TAS)	RTL REG_SH_* (SOURCED)
Credit-based shaper	802.1Qav, hi/lo credit, idle/send slope	RTL REG_SH_* (SOURCED)
Queues	4, strict-priority	kit (SOURCED)
PTP	802.1AS/1588 timestamp: egress/ingress capture, residence, adjust	RTL REG_PTP_/TS_ (SOURCED)
Datapath	8-bit MII (mii_txd/rxd) to off-chip PHY	RTL:208–211 (SOURCED)
Payload buffer	PAYLOAD_BYTES = 256 (default)	RTL:198 (SOURCED)
Interrupt	1 aggregated line (irq_o)	RTL:214 (SOURCED)
Verification	21/21 assertion-based tests	kit (SOURCED)

Top-level block diagram



Standards compliance

- IEEE **802.3** (MAC) · **802.1Qbv** (TAS) · **802.1Qav** (CBS) · **802.1AS / 1588** (PTP). Detail: [[docs/datasheets/aveth/DSHT-02-FEATURES-COMPLIANCE|DSHT-02]].

Source cross-refs

- RTL: rtl/aveth/zen_aveth.sv · Kit: [[docs/kits/AVETH-LICENSE-KIT|AVETH-LICENSE-KIT]] · Catalog: [[docs/catalog/IP-CATALOG-11-AUTOMOTIVE|vol. 11]].

DSHT-01 · AVETH · product overview.

title: “Automotive Ethernet MAC + TSN — Key Features & Standards Compliance”

DSHT-02 · Key Features & Standards Compliance

Scope. Feature matrix + TSN standards-compliance checklist. Distills rtl/aveth/zen_aveth.sv.

Feature matrix

Feature	Supported	Notes	Source
802.3 MAC framing		preamble/SFD (0x55/0xD5), min 64B frame	RTL:234–235,232
CRC-32 FCS (gen + check)		TX append, RX verify	RTL
MAC address filter		DST match to programmed MAC	RTL REG_MAC/DST
Loopback		via CTRL	RTL REG_CTRL
802.1Qbv time-aware shaper		gate-control list (GCL), TAS base/timer, gate vector	RTL REG_SH_GCL/TAS/GATES
802.1Qav credit-based shaper		4 queues, hi/lo credit, idle/send slope, eligibility	RTL REG_SH_Q/CRED
802.1AS/1588 PTP		free-running time, rate incr, offset adjust, TX/RX TS capture, residence	RTL REG_PTP_/TS_
CRC OK/ERR + filter counters		telemetry	RTL REG_*_CNT
Strict-priority 4-queue scheduling			kit
Cut-through / switching		endpoint, not a switch	kit

Standards compliance

Standard	Scope	Status
IEEE 802.3	MAC framing, FCS, addressing	
IEEE 802.1Qbv	time-aware shaper / scheduled traffic	
IEEE 802.1Qav	credit-based shaper	
IEEE 802.1AS / 1588	PTP timestamping / transparent-clock residence	(endpoint scope)

Notes

- PHY is off-chip (MII); no PCS/PMA or SerDes in scope.

Source cross-refs

- RTL: rtl/aveth/zen_aveth.sv (REG_* block @311–369).

DSHT-02 · AVETH · features & compliance.

DSHT-03 · Applications / Use Models

Scope. Target deployments and use models for the Zen AVETH.

Target applications

- **Zonal / SOA backbone** — the bounded-latency in-vehicle network trunk connecting zonal controllers.
- **ADAS / sensor aggregation** — scheduled, time-critical sensor traffic with PTP-aligned timestamps.
- **Legacy-bus bridging** — CAN/LIN/SENT/FlexRay endpoints bridged onto Ethernet via the host.

Use models

- **Scheduled traffic (Qbv)** — program a gate-control list so critical queues open in protected windows; align to the PTP time base for network-wide determinism.
- **Rate-limited streams (Qav)** — credit-based shaping for A/V or telemetry classes that need bandwidth guarantees without starving best-effort.
- **PTP time sync** — hardware egress/ingress timestamps and residence-time for transparent-clock participation.

Recommended companions

- [\[\[docs/catalog/IP-CATALOG-02-INTERRUPTS|Interrupt controller\]\]](#) · [\[\[docs/catalog/IP-CATALOG-01-BUS-FABRIC|Bus Fabric\]\]](#) · [\[\[docs/catalog/IP-CATALOG-11-AUTOMOTIVE|CAN/LIN/FlexRay\]\]](#) for bridged legacy traffic.

Source cross-refs

- Kit: [\[\[docs/kits/AVETH-LICENSE-KIT|AVETH-LICENSE-KIT\]\]](#).

DSHT-03 · AVETH · applications.

title: “Automotive Ethernet MAC + TSN — Configurable Options” created: 2026-09-14 status: authored (pending review) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-04 · Configurable Options

Scope. Build-time parameters and run-time (register) options. Distills `rtl/aveth/zen_aveth.sv`.

Build-time parameters

Source: RTL module header `zen_aveth` — *SOURCED*.

Parameter	Type	Default	Description
PAYLOAD_BYTES	int unsigned	256	TX/RX payload buffer size in bytes. Default keeps sim tractable; size to the largest frame payload required.

Derived widths (localparams, informational)

- `MIN_PAYLOAD` = 46 (min payload for a 64B min frame) · `PREAMBLE_BYTE` = 0x55 · `SFD_BYTE` = 0xD5 (RTL:232–235).

Run-time options (register-selected)

- **MAC identity / filtering** — `REG_MAC_LO/HI`, `REG_DST_`, `REG_SRC_`, `REG_ETYPE`.
- **TAS (Qbv)** — `REG_SH_CTRL/ARM`, GCL length/index/entry, TAS base/timer, gate vector.
- **CBS (Qav)** — per-queue index/len, idle/send slope, hi/lo credit, eligibility.
- **PTP** — `REG_PTP_CTRL/INCR`, time, adjust; TS capture registers.

- Full field detail: [[docs/datasheets/aveth/DSHT-10-REGISTER-MAPIDSHT-10]].

Source cross-refs

- RTL: rtl/aveth/zen_aveth.sv:198,232–235,311–369.

DSHT-04 · AVETH · configurable options.

title: “Automotive Ethernet MAC + TSN — Functional Overview” created: 2026-09-14 status: authored (pending review) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-05 · Functional Overview

Scope. Black-box behavior of the four functions — MAC, 802.1Qbv TAS, 802.1Qav CBS, and PTP. Product altitude; internals summarized, not duplicated. Distills rtl/aveth/zen_aveth.sv.

MAC (802.3)

- **TX:** software stages a frame (DST/SRC/EtherType + payload via the DATA window), sets length, and triggers TX. The MAC prepends preamble (0x55) + SFD (0xD5), transmits over MII, and appends a CRC-32 **FCS**. Frames are padded to the 64-byte minimum (MIN_PAYLOAD=46).
- **RX:** the MAC deframes from MII, verifies FCS, applies the destination-address filter, and exposes the received DST/SRC/EtherType + payload window plus length. CRC-OK / CRC-ERR / filtered counters accumulate.

Time-aware shaper — 802.1Qbv (TAS)

- A **gate-control list (GCL)** of entries (gate vector + interval) is programmed (SH_GCL_LEN/IDX/ENT) and armed (SH_ARM) against a **TAS base time** and timer.
- At run time the gate vector (SH_GATES) opens/closes per-queue transmission windows, aligned to the PTP time base — this is what delivers bounded latency for scheduled traffic.

Credit-based shaper — 802.1Qav (CBS)

- Per-queue (SH_Q_IDX) credit accumulates at an **idle slope** and depletes at a **send slope**; hi/lo credit limits and an **eligibility** function gate transmission. Smooths bursty class traffic without starving best-effort.

PTP — 802.1AS / 1588

- A free-running timer (PTP_TIME_LO/HI) advances by a programmable **increment** (PTP_INCR) each tick; an **adjust** (PTP_ADJ_*) applies offset/rate correction.
- Hardware captures **egress** and **ingress** timestamps (TS_TX_, TS_RX_) SFD-aligned, and a **residence** value (TS_RESID) for transparent-clock operation. Event-frame recognition drives the capture.

Interrupt aggregation

- Enabled sources (REG_IE) set pending bits (REG_IP); the aggregate drives the single irq_o.

Source cross-refs

- RTL: rtl/aveth/zen_aveth.sv (MAC + REG_SH_* TAS/CBS + REG_PTP_/TS_@339–369).

DSHT-05 · AVETH · functional overview.

title: “Automotive Ethernet MAC + TSN — Interfaces & Signals” created: 2026-09-14 status: authored (pending review) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-06 · Interfaces & Signals

Scope. Top-level interfaces of zen_aveth by group. Every port RTL-sourced from rtl/aveth/zen_aveth.sv. Full port table in [[docs/datasheets/aveth/DSHT-A-APPENDICES|App A]].

Interface groups

Group	Signals	Description
Clock / reset	clk_i, rst_ni	single clock; active-low async reset
Peripheral bus	req_i : periph_req_t, rsp_o : periph_rsp_t	struct-typed register access
MII TX	mii_txd_o[7:0], mii_tx_en_o	8-bit MII transmit to off-chip PHY
MII RX	mii_rxd_i[7:0], mii_rx_dv_i	8-bit MII receive from off-chip PHY
Interrupt	irq_o	single aggregated interrupt

Port table (RTL-sourced)

Source: rtl/aveth/zen_aveth.sv:200–214 — SOURCED.

Direction	Signal	Type / width	Notes
input	clk_i	logic	reference clock
input	rst_ni	logic	active-low reset
input	req_i	periph_req_t	bus request
output	rsp_o	periph_rsp_t	bus response
output	mii_txd_o	logic [7:0]	MII transmit data
output	mii_tx_en_o	logic	MII transmit enable
input	mii_rxd_i	logic [7:0]	MII receive data
input	mii_rx_dv_i	logic	MII receive data-valid
output	irq_o	logic	aggregated interrupt

Standards compliance

- MII datapath per IEEE 802.3; register access per the struct-typed peripheral bus (APB4/AXI4-Lite frontends available via [[docs/catalog/IP-CATALOG-01-BUS-FABRIC|Bus Fabric]]).

Source cross-refs

- RTL: rtl/aveth/zen_aveth.sv:200–214.

DSHT-06 · AVETH · interfaces & signals.

title: “Automotive Ethernet MAC + TSN — Clocking & Reset” created: 2026-09-14
status: authored (pending review) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-07 · Clocking & Reset

Scope. Clock/reset requirements and the PTP time base. Distills rtl/aveth/zen_aveth.sv.

Clocking

Item	Spec	Source
Clock inputs	1 (clk_i)	RTL:200 (SOURCED)
Clock domains	single synchronous domain (MII referenced to clk_i)	RTL
PTP time base	derived from clk_i via programmable increment (PTP_INCR)	RTL REG_PTP_INCR
MII rate / fmax	TBC (owner: PD)	—

Reset

Item	Spec	Source
Reset input	rst_ni, active-low	RTL:201 (SOURCED)
Post-reset state	TX/RX idle, GCL disarmed, PTP timer 0, counters 0, registers at reset values	RTL

PTP note

- The PTP timer advances by REG_PTP_INCR per clk_i tick; nominal resolution/accuracy is set by the increment and clock — see [[docs/datasheets/aveth/DSHT-11-PERFORMANCE|DSHT-11]]. Rate/offset corrected via REG_PTP_ADJ_*.

Source cross-refs

- RTL: rtl/aveth/zen_aveth.sv:200–201, REG_PTP_* @357–362.

DSHT-07 · AVETH · clocking & reset.

title: “Automotive Ethernet MAC + TSN — Power-On / Reset / Init Sequence”
created: 2026-09-14 status: authored (pending review) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-08 · Power-On / Reset / Init Sequence

Scope. Bring-up ordering the integrator must drive.

Init sequence

1. Release rst_ni. TX/RX idle, PTP timer 0, GCL disarmed.
2. **MAC identity**: program REG_MAC_LO/Hi (local MAC), and default DST/SRC/EtherType as needed.
3. **PTP (if used)**: set REG_PTP_INCR, start via REG_PTP_CTRL; apply REG_PTP_ADJ_* for sync.
4. **TAS (Qbv, if used)**: write GCL entries (SH_GCL_LEN/IDX/ENT), set TAS base (SH_TAS_BASE) + timer, then arm (SH_ARM). Gates then follow the list.
5. **CBS (Qav, if used)**: per queue (SH_Q_IDX) program idle/send slope + hi/lo credit, set eligibility.
6. **Interrupts**: enable sources in REG_IE; route irq_o.
7. Ready — TX via the frame-staging registers + TXCTRL; RX via the RX window + STATUS.

Notes

- TAS must be armed against a valid PTP/base time for scheduled traffic to align; leave disarmed for best-effort-only operation.

Source cross-refs

- Register detail: [[docs/datasheets/aveth/DSHT-10-REGISTER-MAP|DSHT-10]] · RTL: rtl/aveth/zen_aveth.sv.

DSHT-08 · AVETH · power-on / reset / init.

title: “Automotive Ethernet MAC + TSN — Programming Model” created: 2026-09-14 status: authored (pending review) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-09 · Programming Model

Scope. Register-access model and canonical sequences (TX/RX, GCL, CBS, PTP). Distills rtl/aveth/zen_aveth.sv.

Access model

- Word registers selected by a 6-bit index (REG_*), byte offset = index × 4, spanning 0x00–0xF0.
- The frame payload is accessed through a **windowed** register: set the byte index (REG_DATA_IDX / REG_RXDATA_IDX) then read/write the data window (REG_DATA_WIN / REG_RXDATA_WIN).

Transmit a frame

```
write REG_DST_LO/HI, REG_SRC_LO/HI, REG_ETYPE
for each payload chunk: set REG_DATA_IDX; write REG_DATA_WIN
write REG_TXLEN = payload length
write REG_TXCTRL = start
poll REG_STATUS for TX-done (or take irq_o)
```

Receive a frame

```
on irq_o / poll REG_STATUS for RX-valid
read REG_RXLEN, REG_RX_DST/SRC/ETYPE
for each chunk: set REG_RXDATA_IDX; read REG_RXDATA_WIN
check CRC via REG_CRC_OK_CNT / REG_CRC_ERR_CNT
```

Program the Qbv gate-control list

```
write REG_SH_GCL_LEN = N
for i in 0..N-1: write REG_SH_GCL_IDX=i; write REG_SH_GCL_ENT = {gate_vector, interval}
write REG_SH_TAS_BASE / REG_SH_TAS_TMR
write REG_SH_ARM = 1 # gates now follow the list; REG_SH_GATES reflects live vector
```

Program the Qav credit-based shaper (per queue)

```
write REG_SH_Q_IDX = q
write REG_SH_IDLE = idleSlope; REG_SH_SEND = sendSlope
write REG_SH_HICRED / REG_SH_LOCREC
(read REG_SH_CREDIT / REG_SH_ELIG for state)
```

PTP

```
write REG_PTP_INCR; write REG_PTP_CTRL = enable
adjust: write REG_PTP_ADJ_LO/HI
read timestamps: REG_TS_TX_LO/.., REG_TS_RX_.., REG_TS_RESID
```

Source cross-refs

- Register map: [\[\[docs/datasheets/aveth/DSHT-10-REGISTER-MAP|DSHT-10\]\]](#) · RTL: [rtl/aveth/zen_aveth.sv:311–369](#).

DSHT-09 · AVETH · programming model.

title: “Automotive Ethernet MAC + TSN — Register Map” created: 2026-09-14
status: authored (pending review) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-10 · Register Map

Scope. Full CSR map. Offsets are RTL-sourced from the REG_* localparams in [rtl/aveth/zen_aveth.sv](#) (byte offset = index × 4).

MAC / frame block (0x00–0x64)

Source: [rtl/aveth/zen_aveth.sv:311–336](#) — *SOURCED*.

Offset	Name	Access	Function
0x00	CTRL	R/W	Global control (enable, loopback)
0x04	MAC_LO	R/W	Local MAC address [31:0]
0x08	MAC_HI	R/W	Local MAC address [47:32]
0x0C	DST_LO	R/W	TX destination MAC [31:0]
0x10	DST_HI	R/W	TX destination MAC [47:32]
0x14	SRC_LO	R/W	TX source MAC [31:0]
0x18	SRC_HI	R/W	TX source MAC [47:32]
0x1C	ETYPE	R/W	TX EtherType
0x20	TXLEN	R/W	TX payload length
0x24	DATA_IDX	R/W	TX payload byte index (window ptr)
0x28	DATA_WIN	R/W	TX payload data window
0x2C	TXCTRL	R/W	TX trigger/control
0x30	STATUS	R	TX/RX status flags
0x34	RXLEN	R	RX payload length
0x38	RX_DST_LO	R	RX destination MAC [31:0]
0x3C	RX_DST_HI	R	RX destination MAC [47:32]
0x40	RX_SRC_LO	R	RX source MAC [31:0]
0x44	RX_SRC_HI	R	RX source MAC [47:32]
0x48	RX_ETYPE	R	RX EtherType
0x4C	RXDATA_IDX	R/W	RX payload byte index (window ptr)
0x50	RXDATA_WIN	R	RX payload data window
0x54	CRC_OK_CNT	R	CRC-OK frame counter
0x58	CRC_ERR_CNT	R	CRC-error frame counter
0x5C	FILT_CNT	R	Address-filtered frame counter
0x60	IE	R/W	Interrupt enable
0x64	IP	R/W1C	Interrupt pending

Time-aware shaper — 802.1Qbv (0x80–0x9C)

Source: rtl/aveth/zen_aveth.sv:339–347 — SOURCED.

Offset	Name	Access	Function
0x80	SH_CTRL	R/W	Shaper control
0x84	SH_ARM	R/W	Arm the gate-control list
0x88	SH_GCL_LEN	R/W	GCL length (# entries)
0x8C	SH_GCL_IDX	R/W	GCL entry index
0x90	SH_GCL_ENT	R/W	GCL entry (gate vector + interval)
0x94	SH_TAS_BASE	R/W	TAS base time
0x98	SH_TAS_TMR	R/W	TAS timer
0x9C	SH_GATES	R	Live gate vector

Credit-based shaper — 802.1Qav (0xA0–0xBC)

Source: rtl/aveth/zen_aveth.sv:347–354 — SOURCED.

Offset	Name	Access	Function
0xA0	SH_Q_IDX	R/W	Queue select
0xA4	SH_QLEN	R	Queue occupancy
0xA8	SH_IDLE	R/W	Idle slope
0xAC	SH_SEND	R/W	Send slope
0xB0	SH_HICRED	R/W	Hi-credit limit
0xB4	SH_LOCRED	R/W	Lo-credit limit
0xB8	SH_CREDIT	R	Current credit
0xBC	SH_ELIG	R	Eligibility state

PTP — 802.1AS / 1588 (0xC0–0xF0)

Source: rtl/aveth/zen_aveth.sv:357–369 — SOURCED.

Offset	Name	Access	Function
0xC0	PTP_CTRL	R/W	PTP control (enable)
0xC4	PTP_INCR	R/W	Timer increment per tick
0xC8	PTP_TIME_LO	R/W	PTP time [31:0]
0xCC	PTP_TIME_HI	R/W	PTP time [63:32]
0xD0	PTP_ADJ_LO	R/W	Time adjust [31:0]
0xD4	PTP_ADJ_HI	R/W	Time adjust [63:32]
0xD8	TS_TX_LO	R	TX timestamp [31:0]
0xEC	TS_RX_STAT	R	RX timestamp status
0xF0	TS_RESID	R	Residence time (transparent clock)

Additional TX/RX timestamp high/low registers occupy the 0xDC–0xE8 range (TS_TX_HI, TS_RX_LO/HI); exact field encodings and reset values are TBC (owner: verif) where not asserted in RTL. Index constants: rtl/aveth/zen_aveth.sv:363–368.

Source cross-refs

- Register localparams: rtl/aveth/zen_aveth.sv:311–369.

DSHT-10 · AVETH · register map.

title: “Automotive Ethernet MAC + TSN — Performance” created: 2026-09-14
status: authored (pending review) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-11 · Performance

Scope. Throughput, latency, and PTP resolution envelope. Values not fixed by the standard are TBC.

Throughput

Metric	Value	Source
Line datapath	8-bit MII per clk_i	RTL:208–211
Line rate	MI1-rate dependent (PHY)	TBC (verif)
Max frame payload	PAYLOAD_BYTES (256 default)	RTL:198
Min frame	64 bytes (46B payload floor)	RTL:232

Latency & determinism

Metric	Value	Source
Scheduled-traffic window	per Qbv GCL entry interval	RTL REG_SH_GCL_ENT
CBS shaping	idle/send slope per queue	RTL REG_SH_IDLE/SEND
Register access	1-cycle registered handshake	RTL

PTP

Metric	Value	Source
Time base width	64-bit (PTP_TIME_LO/HI)	RTL REG_PTP_TIME_*
Resolution	= clk_i period × increment scaling (PTP_INCR)	RTL REG_PTP_INCR
Timestamp capture	SFD-aligned egress/ingress	RTL TS_*
Nominal accuracy	TBC (owner: verif)	—

Source cross-refs

- RTL: rtl/aveth/zen_aveth.sv · Verification: [[docs/datasheets/aveth/DSHT-14-VERIFICATION-DELIVERABLESIDSH14]].

DSHT-11 · AVETH · performance.

title: "Automotive Ethernet MAC + TSN — Physical / Implementation" created: 2026-09-14 status: outline (numbers TBC — not yet characterized) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-12 · Physical / Implementation

Scope. Area, fmax, constraints. Process-/flow-dependent — all TBC pending a PPA run (owner: PD).

Implementation envelope

Metric	Value	Source
Cell area	TBC	owner: PD
Max frequency (fmax)	TBC	owner: PD
Target process	TBC	owner: PD

Synthesis notes

- Struct-typed, no SV interfaces; passes Yosys \$11 synth-check (t:\$d latch=0) — no inferred latches. See [[docs/kits/AVETH-LICENSE-KIT|kit]] compliance statement.
- Payload buffer scales with PAYLOAD_BYTES; area is dominated by the buffer + TAS/CBS/PTP register state.

Source cross-refs

- RTL: rtl/aveth/zen_aveth.sv · Constraints: TBC.

DSHT-12 · AVETH · physical / implementation.

title: "Automotive Ethernet MAC + TSN — RAS & Data Integrity" created: 2026-09-14 status: authored (pending review) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-13 · RAS & Data Integrity

Scope. Error detection, telemetry, and reporting. Distills rtl/aveth/zen_aveth.sv.

Data integrity

Mechanism	Behavior	Source
CRC-32 FCS (TX)	appended to every transmitted frame	RTL
CRC-32 FCS (RX)	verified; failing frames counted, flagged	RTL
Address filter	non-matching frames dropped + counted	RTL

Telemetry counters

Counter	Meaning	Register
CRC_OK_CNT	frames received with valid FCS	0x54
CRC_ERR_CNT	frames received with FCS error	0x58
FILT_CNT	frames dropped by address filter	0x5C

Reporting path

- Enabled events (REG_IE) set pending bits (REG_IP) and raise irq_o; software reads REG_STATUS + counters to classify.
- No ECC on the internal payload buffer (not required at this altitude).

Source cross-refs

- RTL: rtl/aveth/zen_aveth.sv (counter + IRQ block) · Registers:

DSHT-13 · AVETH · RAS & data integrity.

title: "Automotive Ethernet MAC + TSN — Verification & Deliverables" created: 2026-09-14 status: authored (pending review) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-14 · Verification & Deliverables

Scope. Verification environment and deliverables manifest. Distills the [[docs/kits/AVETH-LICENSE-KIT|AVETH license kit]].

Verification

Item	Value	Source
Methodology	assertion-based cocotb, byte-exact	kit
Test count	21 / 21 passing	kit (SOURCED)
Coverage highlights	MAC framing/FCS, filter, loopback; Qbv GCL gating; Qav credit; PTP TS capture/residence	kit
Gates	Verilator DV + Yosys §11 synth (t:\$dlatch=0)	kit
Shared VIP	periph_codecs.py bus codecs	kit

Deliverables manifest (kit)

- Parameterized RTL: rtl/aveth/zen_aveth.sv.
- Compliance testbenches + shared VIP.
- Integration docs (this datasheet + [[docs/datasheets/aveth/DSHT-15-INTEGRATION-GUIDE|DSHT-15]]).
- Compliance statement (two-gate evidence).

Source cross-refs

- Kit: [[docs/kits/AVETH-LICENSE-KIT|AVETH-LICENSE-KIT]] · Regression: scripts/run-regression.sh.

DSHT-14 · AVETH · verification & deliverables.

title: "Automotive Ethernet MAC + TSN — Integration Guide" created: 2026-09-14 status: authored (pending review) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-15 · Integration Guide

Scope. Instantiation, PHY/MII connection, tie-offs, DFT. Distills rtl/aveth/.

Instantiation

- Instantiate zen_aveth; set PAYLOAD_BYTES to the largest frame payload required (default 256).
- Attach the register port to the host fabric (periph bus, or APB4/AXI4-Lite via [[docs/catalog/IP-CATALOG-01-BUS-FABRIC|Bus Fabric]]).

Connections

Signal	Connect to
clk_i / rst_ni	SoC clock / active-low reset
mii_txd_o / mii_tx_en_o	off-chip Ethernet PHY (MII TX)
mii_rxd_i / mii_rx_dv_i	off-chip Ethernet PHY (MII RX)
irq_o	interrupt controller ([[docs/catalog/IP-CATALOG-02-INTERRUPTSIPLIC/AIA]])

Notes

- **Endpoint MAC, not a switch** — one MII port to one PHY.
- For network-wide determinism, drive the PTP time base from the grandmaster and align the Qbv base time accordingly.
- DFT/scan hooks: TBC (owner: DFT).

Source cross-refs

- RTL: rtl/aveth/zen_aveth.sv · Bridges: [[docs/BRIDGE-INTEGRATION-GUIDE|bridge integration guide]].

DSHT-15 · AVETH · integration guide.

title: “Automotive Ethernet MAC + TSN — Ordering / Licensing / Support” created: 2026-09-14 status: authored (pending review) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-16 · Ordering / Licensing / Support

Scope. Commercial terms. Distills the [[docs/kits/AVETH-LICENSE-KIT|AVETH license kit]].

Product

Item	Value
Kit	zen-aveth-kit-v1 (Wave-B flagship)
Catalog entry	[[docs/catalog/IP-CATALOG-11-AUTOMOTIVE IP-CATALOG vol. 11 · Automotive]]
Deliverable	parameterized RTL + VIP + compliance TB + integration docs + compliance statement

Licensing

- **Internal soft-license** by default; kit is license-ready-structured for external.
- Packaged via scripts/package-kit.sh; kit-eligible only after passing both gates (Verilator DV + Yosys §11).

Support

- Owner: zen-peripheral (RHA: Amanda Chen). Integration questions via the kit contact.

Source cross-refs

- Kit: [[docs/kits/AVETH-LICENSE-KIT|AVETH-LICENSE-KIT]] · Licensing model: [[docs/catalog/IP-CATALOG-00-INDEX|catalog index]].

DSHT-16 · AVETH · ordering / licensing / support.

title: “Automotive Ethernet MAC + TSN — Appendices” created: 2026-09-14 status: authored (pending review) standard: shared-agent-infra/DATASHEET-STANDARD.md —

DSHT-A · Appendices

Appendix A — Signal descriptions (full port table)

Source: rtl/aveth/zen_aveth.sv:200–214 — SOURCED.

Signal	Dir	Type	Description
clk_i	in	logic	Reference clock.
rst_ni	in	logic	Active-low asynchronous reset.
req_i	in	periph_req_t	Peripheral-bus request.
rsp_o	out	periph_rsp_t	Peripheral-bus response.
mii_txd_o	out	logic [7:0]	MII transmit data to off-chip PHY.
mii_tx_en_o	out	logic	MII transmit enable.
mii_rxd_i	in	logic [7:0]	MII receive data from off-chip PHY.
mii_rx_dv_i	in	logic	MII receive data-valid.
irq_o	out	logic	Aggregated interrupt.

Appendix B — Acronyms

- **TSN** time-sensitive networking · **TAS** time-aware shaper (802.1Qbv) · **CBS** credit-based shaper (802.1Qav) · **GCL** gate-control list · **PTP** precision time protocol (802.1AS/1588) · **FCS** frame-check sequence · **MII** media-independent interface · **SFD** start-of-frame delimiter.

Appendix C — References

- shared-agent-infra/DATASHEET-STANDARD.md · IEEE 802.3 · 802.1Qbv · 802.1Qav · 802.1AS / 1588.
- Source: rtl/aveth/zen_aveth.sv.

Appendix D — Revision history

Date	Rev	Change	Author
2026-09-14	0.1	Initial datasheet authored from as-built RTL (pilot).	Amanda Chen (RHA)

DSHT-A · AVETH · appendices.